ANALOG DEVICES

LC^2MOS 16-Bit A/D Converter

AD7701

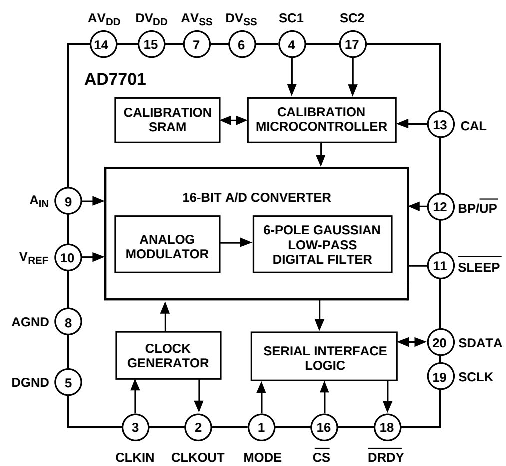
FEATURES

Monolithic 16-Bit ADC
0.0015% Linearity Error
On-Chip Self-Calibration Circuitry
Programmable Low-Pass Filter
0.1 Hz to 10 Hz Corner Frequency
0 V to +2.5 V or ±2.5 V Analog Input Range
4 kSPS Output Data Rate
Flexible Serial Interface
Ultralow Power

APPLICATIONS

Industrial Process Control
Weigh Scales
Portable Instrumentation
Remote Data Acquisition

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7701 is a 16-bit ADC which uses a sigma-delta conversion technique. The analog input is continuously sampled by an analog modulator whose mean output duty cycle is proportional to the input signal. The modulator output is processed by an on-chip digital filter with a six-pole Gaussian response, which updates the output data register with 16-bit binary words at word rates up to 4 kHz. The sampling rate, filter corner frequency and output word rate are set by a master clock input that may be supplied externally, or by a crystal-controlled on-chip clock oscillator.

The inherent linearity of the ADC is excellent, and endpoint accuracy is ensured by self-calibration of zero and full scale which may be initiated at any time. The self-calibration scheme can also be extended to null system offset and gain errors in the input channel.

The output data is accessed through a flexible serial port, which has an asynchronous mode compatible with UARTs and two synchronous modes suitable for interfacing to shift registers or the serial ports of industry-standard microcontrollers.

CMOS construction insures low power dissipation, and a power down mode reduces the idle power consumption to only 10 μW.

PRODUCT HIGHLIGHTS

1. The AD7701 offers 16-bit resolution coupled with outstanding 0.0015% accuracy.
2. No missing codes ensures true, usable, 16-bit dynamic range, removing the need for programmable gain and level-setting circuitry.
3. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero and gain error. External circuits can also be included in the calibration loop to remove system offsets and gain errors.
4. A flexible synchronous/asynchronous interface allows the AD7701 to interface directly to UARTs or to the serial ports of industry-standard microcontrollers.
5. Low operating power consumption and an ultralow power standby mode make the AD7701 ideal for loop-powered remote sensing applications, or battery-powered portable instruments.

REV. D

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AD7701–SPECIFICATIONS

(T_A = +25°C; AV_{DD} = DV_{DD} = +5 V; AV_{SS} = DV_{SS} = –5 V; V_{REF} = +2.5 V; f_{CLKIN} = 4.096 MHz; Bipolar Mode: MODE = +5 V; A_{IN} Source Resistance = 1k Ω[1] with 1 nF to AGND at A_{IN}, unless otherwise noted.)

Parameter	A, S Versions[2]	B, T Versions[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	16	16	Bits	
Integral Nonlinearity				
T_{MIN} to T_{MAX}		±0.0007	% FSR typ	
	±0.003	±0.0015	% FSR max	
Differential Nonlinearity				
T_{MIN} to T_{MAX}	±0.125	±0.125	LSB typ	Guaranteed No Missing Codes
	±0.5	±0.5	LSB max	
Positive Full-Scale Error[3]	±0.13	±0.13	LSB typ	
	±0.5	±0.5	LSB max	
Full-Scale Drift[4]	±1.2 (±2.3 S Version)	±1.2 (±2.3 T Version)	LSB typ	
Unipolar Offset Error[3]	±0.25	±0.25	LSB typ	
	±1	±1	LSB max	
Unipolar Offset Drift[4]	±1.6 (+3/–25 S Version)	±1.6 (+3/–25 T Version)	LSB typ	
Bipolar Zero Error[3]	±0.25	±0.25	LSB typ	
	±1	± 1	LSB max	
Bipolar Zero Drift[4]	±0.8 (+1.5/–12.5 S Version)	±0.8 (+1.5/–12.5 T Version)	LSB typ	
Bipolar Negative Full-Scale Error[3]	±0.5	±0.5	LSB typ	
	±2	±2	LSB max	
Bipolar Negative Full-Scale Drift[4]	±0.6 (±1.2 S Version)	±0.6 (±1.2 T Version)	LSB typ	
Noise (Referred to Output)	0.1	0.1	LSB rms typ	
DYNAMIC PERFORMANCE				
Sampling Frequency, f_S	f_{CLKIN}/256	f_{CLKIN}/256	Hz	
Output Update Rate, f_{OUT}	f_{CLKIN}/1024	f_{CLKIN}/1024	Hz	
Filter Corner Frequency, $f_{-3\ dB}$	f_{CLKIN}/409,600	f_{CLKIN}/409,600	Hz	
Settling Time to ±0.0007% FS	507904/f_{CLKIN}	507904/f_{CLKIN}	sec	For Full-Scale Input Step
SYSTEM CALIBRATION				Applies to Unipolar and
Positive Full-Scale Overrange	V_{REF} + 0.1	V_{REF} + 0.1	V max	Bipolar Ranges. After Cali-
Positive Full-Scale Overrange	V_{REF} + 0.1	V_{REF} + 0.1	V max	bration, If A_{IN} > V_{REF}, the
Negative Full-Scale Overrange	–(V_{REF} + 0.1)	–(V_{REF} + 0.1)	V max	Device Will Output All 1s
Maximum Offset Calibration Range[5, 6]				If A_{IN} < 0 (Unipolar) or
Unipolar Input Range	–(V_{REF} + 0.1)	–(V_{REF} + 0.1)	V max	–V_{REF} (Bipolar), the Device
Bipolar Input Range	–0.4 V_{REF} to +0.4 V_{REF}	–0.4 V_{REF} to +0.4 V_{REF}	V max	Will Output All 0s.
Input Span[7]	0.8 V_{REF}	0.8 V_{REF}	V min	
	2 V_{REF} + 0.2	2 V_{REF} + 0.2	V max	
ANALOG INPUT				
Unipolar Input Range	0 to +2.5	0 to +2.5	Volts	
Bipolar Input Range	±2.5	±2.5	Volts	
Input Capacitance	10	10	pF typ	
Input Bias Current[1]	1	1	nA typ	
LOGIC INPUTS				
All Inputs Except CLKIN				
V_{INL}, Input Low Voltage	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.0	2.0	V min	
CLKIN				
V_{INL}, Input Low Voltage	0.8	0.8	V max	
V_{INH}, Input High Voltage	3.5	3.5	V min	
I_{IN}, Input Current	10	10	µA max	
LOGIC OUTPUTS				
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	DV_{DD} – 1	DV_{DD} – 1	V min	I_{SOURCE} = 100 µA
Floating State Leakage Current	±10	±10	µA max	
Floating State Output Capacitance	9	9	pF typ	

Parameter	A, S Versions[2]	B, T Versions[2]	Units	Test Conditions/Comments
POWER REQUIREMENTS[8]				
Power Supply Voltages				
Analog Positive Supply (AV_{DD})	4.5/5.5	4.5/5.5	V min/V max	
Digital Positive Supply (DV_{DD})	4.5/AV_{DD}	4.5/AV_{DD}	V min/V max	
Analog Negative Supply (AV_{SS})	–4.5/–5.5	–4.5/–5.5	V min/V max	
Digital Negative Supply (DV_{SS})	–4.5/–5.5	–4.5/–5.5	V min/V max	
Calibration Memory Retention				
Power Supply Voltage	2.0	2.0	V min	
DC Power Supply Currents[8]				
Analog Positive Supply (AI_{DD})	3.2	3.2	mA max	Typically 2 mA
Digital Positive Supply (DI_{DD})	1.5	1.5	mA max	Typically 1 mA
Analog Negative Supply (AI_{SS})	3.2	3.2	mA max	Typically 2 mA
Digital Negative Supply (DI_{SS})	0.1	0.1	mA max	Typically 0.03 mA
Power Supply Rejection[9]				
Positive Supplies	70	70	dB typ	
Negative Supplies	75	75	dB typ	
Power Dissipation				
Normal Operation	40	40	mW max	$\overline{SLEEP}$ = Logic 1, Typically 25 mW
Standby Operation[10]	20 (40 S Version)	20 (40 T Version)	µW max	$\overline{SLEEP}$ = Logic 0, Typically 10 µW

NOTES

[1]The A_{IN} pin presents a very high impedance dynamic load which varies with clock frequency.

[2]Temperature ranges are as follows: A, B Versions; –40°C to +85°C; S, T Versions; –55°C to +125°C.

[3]Apply after calibration at the temperature of interest. Full-scale error applies for both unipolar and bipolar input ranges.

[4]Total drift over the specified temperature range since calibration at power-up at +25°C. This is guaranteed by design and/or characterization. Recalibration at any temperature will remove these errors.

[5]In unipolar mode the offset can have a negative value ($-V_{REF}$) such that the unipolar mode can mimic bipolar mode operation.

[6]The specifications for input overrange and for input span apply additional constraints on the offset calibration range.

[7]For unipolar mode, input span is the difference between full scale and zero scale. For bipolar mode, input span is the difference between positive and negative full-scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of $\pm(V_{REF}$ +0.1)

[8]All digital outputs unloaded. All digital inputs at 5 V CMOS levels.

[9]Applies in 0.1 Hz to 10 Hz bandwidth. PSRR at 60 Hz will exceed 120 dB due to the digital filter.

[10]CLKIN is stopped. All digital inputs are grounded.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

DV_{DD} to AGND . . . . –0.3 V to +6 V
DV_{DD} to AV_{DD} . . . . –0.3 V to +0.3 V
DV_{SS} to AGND . . . . +0.3 V to –6 V
AV_{DD} to AGND . . . . –0.3 V to +6 V
AV_{SS} to AGND . . . . +0.3 V to –6 V
AGND to DGND . . . . –0.3 V to +0.3 V
Digital Input Voltage to DGND . . . . –0.3 V to DV_{DD} +0.3 V
Analog Input
Voltage to AGND . . . . AV_{SS} – 0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] . . . . ±10 mA
Operating Temperature Range
Commercial Plastic (A, B Versions) . . . . . –40°C to +85°C
Industrial Cerdip (A, B Versions) . . . . –40°C to +85°C
Extended Cerdip (S, T Versions) . . . . . . –55°C to +125°C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . 450 mW
Derates above +75°C by . . . . 10 mW/°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

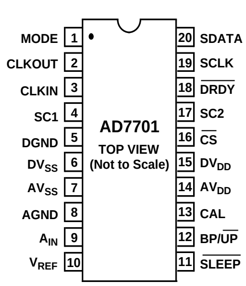


PIN FUNCTION DESCRIPTION

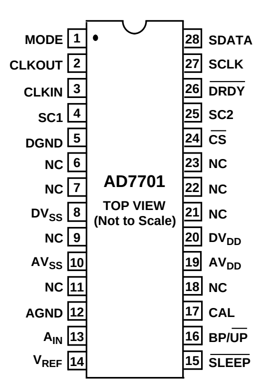
Pin	Mnemonic	Description
1	MODE	Selects the Serial Interface Mode. If MODE is tied to –5 V, the AD7701 will operate in the asynchronous communications (ac) mode. The SCLK pin is configured as an input, and data is transmitted in two bytes, each with one start bit and two stop bits. If MODE is tied to DGND, the synchronous external clocking (SEC) mode is selected. SCLK is configured as an input, and the output appears without formatting, the MSB coming first. If MODE is tied to +5 V, the AD7701 operates in the synchronous self-clocking (SSC) mode. SCLK is configured as an output, with a clock frequency of $f_{CLKIN}/4$ and 25% duty-cycle.
2	CLKOUT	Clock Output to generate an Internal Master Clock by connecting a crystal between CLKOUT and CLKIN. If an external clock is used, CLKOUT is not connected.
3	CLKIN	Clock Input for External Clock.
4, 17	SC1, SC2	System Calibration Pins. The state of these pins, when CAL is taken high, determines the type of calibration performed.
5	DGND	Digital Ground. Ground reference for all digital signals.
6	DV_{SS}	Digital Negative Supply, –5 V nominal.
7	AV_{SS}	Analog Negative Supply, –5 V nominal.
8	AGND	Analog Ground. Ground reference for all analog signals.
9	A_{IN}	Analog Input.
10	V_{REF}	Voltage Reference Input, +2.5 V nominal. This determines the value of positive full-scale in the unipolar mode and of both positive and negative full-scale in the bipolar mode.
11	$\overline{SLEEP}$	Sleep mode pin. When this pin is taken low, the AD7701 goes into a low-power mode with typically 10 μW power consumption.
12	BP/$\overline{UP}$	Bipolar/Unipolar Mode Pin. When this pin is low, the AD7701 is configured for a unipolar input range going from AGND to V_{REF}. When Pin 12 is high, the AD7701 is configured for a bipolar input range, $\pm V_{REF}$.
13	CAL	Calibration Mode Pin. When CAL is taken high for more than 4 cycles, the AD7701 is reset and performs a calibration cycle when CAL is brought low again. The CAL pin can also be used as a strobe to synchronize the operation of several AD7701s.
14	AV_{DD}	Analog Positive Supply, +5 V nominal.
15	DV_{DD}	Digital Positive Supply, +5 V nominal.
16	$\overline{CS}$	Chip Select Input. When $\overline{CS}$ is brought low, the AD7701 will begin to transmit serial data in a format determined by the state of the MODE pin.
18	$\overline{DRDY}$	Data Ready output. $\overline{DRDY}$ is low when valid data is available in the output register. It goes high after transmission of a word is completed. It also goes high for four clock cycles when a new data word is being loaded into the output register, to indicate that valid data is not available, irrespective of whether data transmission is complete or not.
19	SCLK	Serial Clock Input/Output. The SCLK pin in configured as an input or output, dependent on the type of serial data transmission that has been selected by the MODE pin. When configured as an output in the synchronous self-clocking mode, it has a frequency of $f_{CLKIN}/4$ and a duty cycle of 25%.
20	SDATA	Serial Data Output. The AD7701's output data is available at this pin as a 16-bit serial word. The transmission format is determined by the state of the MODE pin.

PIN CONFIGURATIONS

DIP, Cerdip, SOIC



SSOP



ORDERING GUIDE

Model	Temperature Range	Linearity Error (% FSR)	Package Options*
AD7701AN	–40°C to +85°C	0.003	N-20
AD7701BN	–40°C to +85°C	0.0015	N-20
AD7701AR	–40°C to +85°C	0.003	R-20
AD7701BR	–40°C to +85°C	0.0015	R-20
AD7701ARS	–40°C to +85°C	0.003	RS-28
AD7701AQ	–40°C to +85°C	0.003	Q-20
AD7701BQ	–40°C to +85°C	0.0015	Q-20
AD7701SQ	–55°C to +125°C	0.003	Q-20
AD7701TQ	–55°C to +125°C	0.0015	Q-20

NOTES
*N = Plastic DIP; Q = Cerdip; R = SOIC; RS = SSOP.

TIMING CHARACTERISTICS[1, 2]

($AV_{DD} = DV_{DD} = +5$ V ± 10%; $AV_{SS} = DV_{SS} = –5$ V ± 10%; AGND = DGND = 0 V; f_{CLKIN} = 4.096 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD})

Parameter	Limit at T_{MIN}, T_{MAX} (A, B Versions)	Limit at T_{MIN}, T_{MAX} (S, T Versions)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	200	200	kHz min	Master Clock Frequency: Internal Gate Oscillator
	5	5	MHz max	Typically 4.096 MHz
	200	200	kHz min	Master Clock Frequency: Externally Supplied
	5	5	MHz max	
t_r[5]	50	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	50	ns max	Digital Output Fall Time. Typically 20 ns
t_1	0	0	ns min	SC1, SC2 to CAL High Setup Time
t_2	50	50	ns min	SC1, SC2 Hold Time After CAL Goes High
t_3[6]	1000	1000	ns min	$\overline{SLEEP}$ High to CLKIN High Setup Time
SSC Mode				
t_4[7]	$3/f_{CLKIN}$	$3/f_{CLKIN}$	ns max	Data Access Time ($\overline{CS}$ Low to Data Valid)
t_5	100	100	ns max	SCLK Falling Edge to Data Valid Delay (25 ns typ)
t_6	250	250	ns min	MSB Data Setup Time. Typically 380 ns
t_7	300	300	ns max	SCLK High Pulse Width. Typically 240 ns
t_8	790	790	ns max	SCLK Low Pulse Width. Typically 730 ns
t_9[8]	$1/f_{CLKIN}$ +200	$1/f_{CLKIN}$ +200	ns max	SCLK Rising Edge to Hi-Z Delay ($1/f_{CLKIN}$ + 100 ns typ)
t_{10}[8, 9]	$(4/f_{CLKIN})$ +200	$(4/f_{CLKIN})$ +200	ns max	$\overline{CS}$ High to Hi-Z Delay
SEC Mode				
f_{SCLK}	5	5	MHz	Serial Clock Input Frequency
t_{11}	35	35	ns min	SCLK Input High Pulse Width
t_{12}	160	160	ns min	SCLK Low Pulse Width
t_{13}[7, 10]	160	160	ns max	Data Access Time ($\overline{CS}$ Low to Data Valid). Typically 80 ns
t_{14}[11]	150	150	ns max	SCLK Falling Edge to Data Valid Delay. Typically 75 ns
t_{15}[8]	250	250	ns max	$\overline{CS}$ High to Hi-Z Delay
t_{16}[8]	200	200	ns max	SCLK Falling Edge to Hi-Z Delay. Typically 100 ns
AC Mode				
t_{17}	40	40	ns min	$\overline{CS}$ Setup Time. Typically 20 ns
t_{18}	180	180	ns max	Data Delay Time. Typically 90 ns
t_{19}	200	200	ns max	SCLK Falling Edge to Hi-Z Delay. Typically 100 ns

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 1 to 6.

[3]CLKIN Duty Cycle range is 20% to 80%. CLKIN must be supplied whenever the AD7701 is not in SLEEP mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7701 is production tested with f_{CLKIN} at 4.096 MHz. It is guaranteed by characterization to operate at 200 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]In order to synchronize several AD7701s together using the $\overline{SLEEP}$ pin, this specification is met.

[7]t_4 and t_{13} are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[8]t_9, t_{10}, t_{15} and t_{16} are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the Timing Characteristics is the true bus relinquish time of the part and as such as independent of external bus loading capacitance.

[9]If $\overline{CS}$ is returned high before all 16 bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

[10]If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for four clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, the SCLK input should not be taken high sooner than 4 CLKIN cycles plus 160 ns after $\overline{CS}$ goes low.

[11]SDATA is clocked out on the falling edge of the SCLK input.

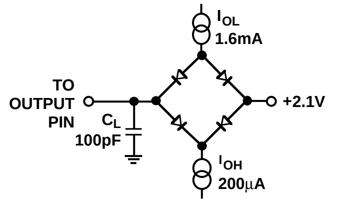


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

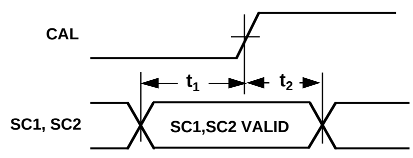


Figure 2a. Calibration Control Timing

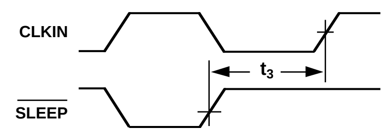


Figure 2b. $\overline{SLEEP}$ Mode Timing

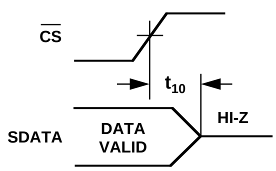


Figure 3. SSC Mode Data Hold Time

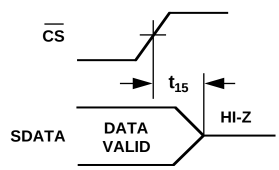


Figure 4a. SEC Mode Data Hold Time

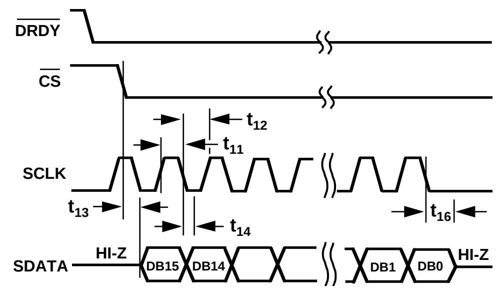


Figure 4b. SEC Mode Timing Diagram

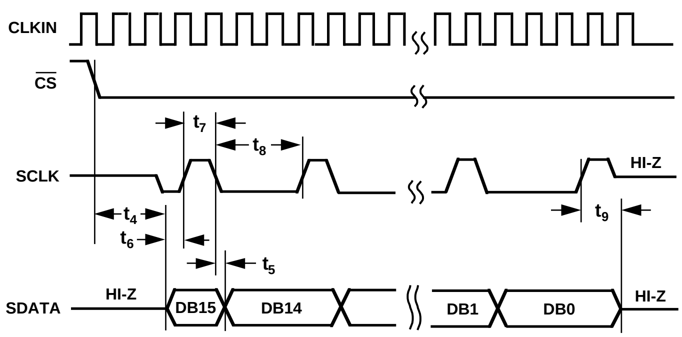


Figure 5. SSC Mode Timing Diagram

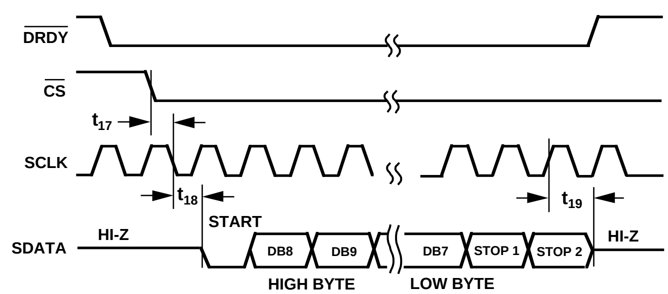


Figure 6. AC Mode Timing Diagram

TERMINOLOGY

LINEARITY ERROR

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are Zero-Scale (not to be confused with Bipolar Zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and Full-Scale, a point 1.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

DIFFERENTIAL LINEARITY ERROR

This is the difference between any code's actual width and the ideal (1 LSB) width. Differential Linearity Error is expressed in LSBs. A differential linearity specification of ±1 LSB or less guarantees monotonicity.

POSITIVE FULL-SCALE ERROR

Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal (V_{REF} –3/2 LSBs). It applies to both positive and negative analog input ranges and it is expressed in microvolts.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the deviation of the first code transition from the ideal (AGND + 0.5 LSB) when operating in the unipolar mode. It is expressed in microvolts.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal (AGND – 0.5 LSB) when operating in the bipolar mode. It is expressed in microvolts.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal ($-V_{REF}$ + 0.5 LSB), when operating in the bipolar mode. It is expressed in microvolts.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages greater than $+V_{REF}$ (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter. It is expressed in millivolts.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages below $-V_{REF}$ without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode. The overhead is expressed in millivolts.

OFFSET CALIBRATION RANGE

In the system calibration modes (SC2 low) the AD7701 calibrates its offset with respect to the A_{IN} pin. The Offset Calibration Range specification defines the range of voltages, expressed as a percentage of V_{REF} that the AD7701 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7701 can accept in the system calibration mode and still calibrate full-scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7701's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full-scale that the AD7701 can accept and still calibrate gain accurately. The input span is expressed as a percentage of $V_{REF.}$

GENERAL DESCRIPTION

The AD7701 is a 16-bit A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those representing chemical, physical or biological processes. It contains a charge-balancing (sigma-delta) ADC, calibration microcontroller with on-chip static RAM, a clock oscillator and a serial communications port.

The analog input signal to the AD7701 is continuously sampled at a rate determined by the frequency of the master clock, CLKIN. A charge-balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. A six-pole Gaussian digital low-pass filter processes the output of the modulator and updates the 16-bit output register at a 4 kHz rate. The output data can be read from the serial port randomly or periodically at any rate up to 4 kHz.

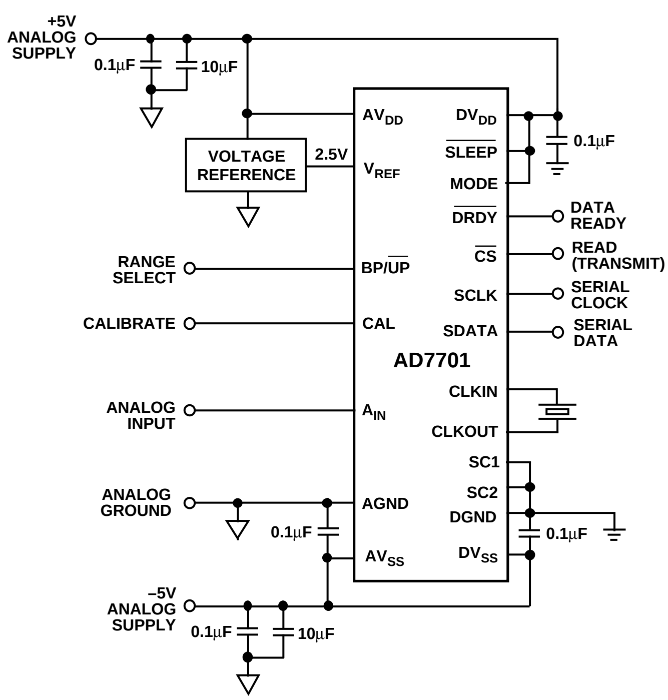


Figure 7. Typical System Connection Diagram

The AD7701 can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. A calibration cycle may be initiated at any time using the CAL control input.

Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel.

For battery operation, the AD7701 also offers a standby mode that reduces idle power consumption to typically 10 µW.

THEORY OF OPERATION

The general block diagram of a sigma-delta ADC is shown in Figure 8. It contains the following elements.

1. A sample-hold amplifier.
2. A differential amplifier or subtracter.
3. An analog low-pass filter.
4. A 1-bit A/D converter (comparator).
5. A 1-bit DAC.
6. A digital low-pass filter.

In operation, the analog signal sample is fed to the subtracter, along with the output of the 1-bit DAC. The filtered difference signal is fed to the comparator, whose output samples the difference signal at a frequency many times that of the analog signal sampling frequency (oversampling).

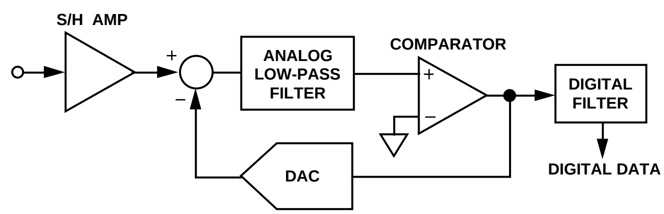


Figure 8. General Sigma-Delta ADC

Oversampling is fundamental to the operation of sigma-delta ADCs. Using the quantization noise formula for an ADC:

$$SNR = (6.02 \times \textit{number of bits} + 1.76)\ dB$$

a 1-bit ADC or comparator yields an SNR of 7.78 dB.

The AD7701 samples the input signal at 16 kHz, which spreads the quantization noise from 0 to 8 kHz. Since the specified analog input bandwidth of the AD7701 is only 0 to 10 Hz, the noise energy in this bandwidth would be only 1/800 of the total quantization noise, even if the noise energy was spread evenly throughout the spectrum. It is reduced still further by analog filtering in the modulator loop, which shapes the quantization noise spectrum to move most of the noise energy to frequencies above 10 Hz. The SNR performance in the 0 to 10 Hz range is conditioned to the 16-bit level in this fashion.

The output of the comparator provides the digital input for the 1-bit DAC, so that the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. It can be retrieved as a parallel binary data word using a digital filter.

Sigma-delta ADCs are generally described by the order of the analog low-pass filter. A simple example of a first order sigma-delta ADC is shown in Figure 9. This contains only a first-order low-pass filter or integrator. It also illustrates the derivation of the alternative name for these devices: Charge-Balancing ADCs.

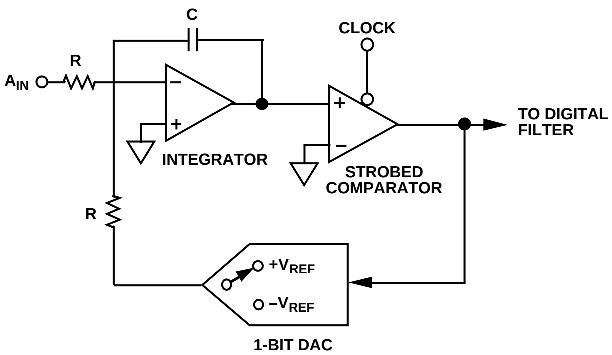


Figure 9. SEC Basic Charge-Balancing ADC

The term charge-balancing comes from the fact that this system is a negative feedback loop that tries to keep the net charge on the integrator capacitor at zero, by balancing charge injected by the input voltage with charge injected by the 1-bit DAC. When the analog input is zero, the only contribution to the integrator output comes from the 1-bit DAC. For the net charge on the integrator capacitor to be zero, the DAC output must spend half its time at +1 V and half its time at –1 V. Assuming ideal components, the duty cycle of the comparator will be 50%.

When a positive analog input is applied, the output of the 1-bit DAC must spend a larger proportion of the time at +1 V, so the duty cycle of the comparator increases. When a negative input voltage is applied, the duty cycle decreases.

The AD7701 uses a second-order sigma-delta modulator and a sophisticated digital filter that provides a rolling average of the sampled output. After power-up or if there is a step change in the input voltage, there is a settling time that must elapse before valid data is obtained.

DIGITAL FILTERING

The AD7701's digital filter behaves like a similar analog filter, with a few minor differences.

First, since digital filtering occurs after the A to D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7701 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 100 mV. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the gain in the input channel so that a full-scale input (2.5 V) gives only a half-scale input to the AD7701 (1.25 V). This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

FILTER CHARACTERISTICS

The cutoff frequency of the digital filter is f_{CLK} /409600. At the maximum clock frequency of 4.096 MHz, the cutoff frequency of the filter is 10 Hz and the output rate is 4 kHz.

Figure 10 shows the filter frequency response. This is a 6-pole Gaussian response that provides 55 dB of 60 Hz rejection for a 10 Hz cutoff frequency. If the clock frequency is halved to give a 5 Hz cutoff, 60 Hz rejection is better than 90 dB. A normalized s-domain pole-zero plot of the filter is shown in Figure 11.

The response of the filter is defined by:

$$H(x) = [1+ 0.693x^2 + 0.240x^4 + 0.0555x^6 + 0.00962x^8 + 0.00133x^{10} + 0.000154x^{12}]^{-0.5}$$

where:

$x = f/f_{3\,dB}$, $f_{3\,dB} = f_{CLKIN}/409600$,

and

f is the frequency of interest.

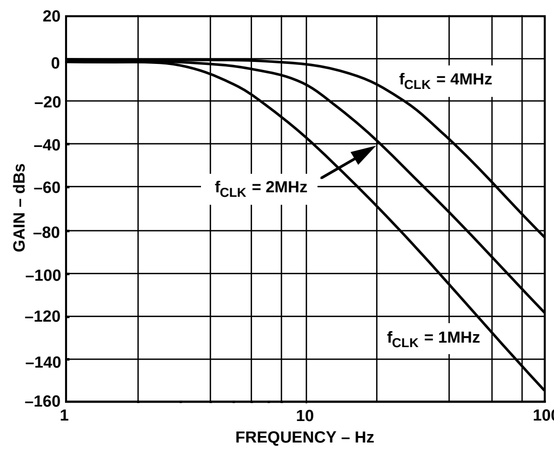


Figure 10. Frequency Response of AD7701 Filter

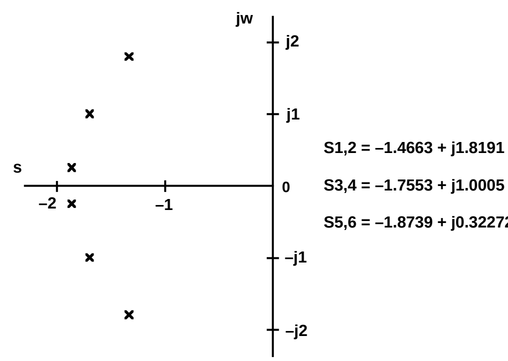


Figure 11. Normalized Pole-Zero Plot of AD7701 Filter

Since the AD7701 contains this on-chip, low-pass filtering, there is a settling time associated with step function inputs, and data will be invalid after a step change until the settling time has elapsed. The AD7701 is therefore unsuitable for high speed multiplexing, where channels are switched and converted sequentially at high rates, as switching between channels can cause a step change in the input. Rather, it is intended for distributed converter systems using one ADC per channel.

However, slow multiplexing of the AD7701 is possible, provided that the settling time is allowed to elapse before data for the new channel is accessed.

The output settling of the AD7701 in response to a step input change is shown in Figure 12. The Gaussian response has fast settling with no overshoot, and the worst-case settling time to ±0.0007% (±0.5 LSB) is 125 ms with a 4.096 MHz master clock frequency.

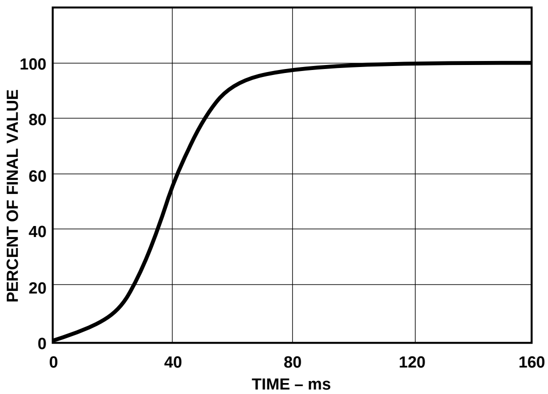


Figure 12. AD7701 Step Response

USING THE AD7701

SYSTEM DESIGN CONSIDERATIONS

The AD7701 operates differently from successive approximation ADCs or other integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The 16-bit output register is updated at a 4 kHz rate, and the output can be read at any time, either synchronously or asynchronously.

CLOCKING

The AD7701 requires a master clock input, which may be an external TTL/CMOS compatible clock signal applied to the CLKIN pin (CLKOUT not used). Alternatively, a crystal of the correct frequency can be connected between CLKIN and CLKOUT, when the clock circuit will function as a crystal-controlled oscillator.

The input sampling frequency, output data rate, filter characteristics and calibration time are all directly related to the master clock frequency f_{CLKIN} by the ratios given in the specification table. Therefore, the first step in system design with the AD7701 is to select a master clock frequency suitable for the bandwidth and output data rate required by the application.

ANALOG INPUT RANGES

The AD7701 performs conversion relative to an externally supplied reference voltage, which allows easy interfacing to ratiometric systems. In addition, either unipolar or bipolar input voltage range may be selected using the BP/$\overline{UP}$ input. With BP/$\overline{UP}$ tied low, the input range is unipolar and the span is 0 to $+V_{REF}$. With BP/$\overline{UP}$ tied high, the input range is bipolar and the span is $\pm V_{REF}$. In the bipolar mode both positive and negative full scale are directly determined by V_{REF}. This offers superior tracking of positive and negative full scale and better midscale (bipolar zero) stability than bipolar schemes that simply scale and offset the input range.

The digital output coding for the unipolar range is Unipolar Binary; for the bipolar range it is Offset Binary. Bit weights for the unipolar and bipolar modes are shown in Table I. The input voltages and output codes for unipolar and bipolar ranges, using the recommended +2.5 V reference, are shown in Table II.

Table I. Bit Weight Table (2.5 V Reference Voltage)

Unipolar Mode				Bipolar Mode		
μV	LSBs	% FS	ppm FS	LSBs	% FS	ppm FS
10	0.26	0.0004	4	0.13	0.0002	2
19	0.5	0.0008	8	0.26	0.0004	4
38	1.00	0.0015	15	0.5	0.0008	8
76	2.00	0.0031	31	1.00	0.0015	15
153	4.00	0.0061	61	2.00	0.0031	31

Table II. Output Coding

Unipolar Mode Input Relative to FS and AGND	Input in Volts	Bipolar Mode Input Relative to FS and AGND	Input in Volts	Output Data
				1111 1111 1111 1111
$+V_{REF}$ – 1.5 LSB	+2.499943	$+V_{REF}$ – 1.5 LSB	+2.499886	1111 1111 1111 1110
$+V_{REF}$ – 2.5 LSB	+2.499905	$+V_{REF}$ – 2.5 LSB	+2.499810	1111 1111 1111 1101
$+V_{REF}$ – 3.5 LSB	+2.499867	$+V_{REF}$ – 3.5 LSB	+2.499733	1111 1111 1111 1100
				1000 0000 0000 0001
$+V_{REF}$/2 + 0.5 LSB	+1.250019	AGND + 0.5 LSB	+0.000038	1000 0000 0000 0000
$+V_{REF}$/2 – 0.5 LSB	+1.249981	AGND – 0.5 LSB	–0.000038	0111 1111 1111 1111
$+V_{REF}$/2 – 1.5 LSB	+1.249943	AGND – 1.5 LSB	–0.000114	0111 1111 1111 1110
				0000 0000 0000 0011
AGND + 2.5 LSB	+0.000095	$-V_{REF}$ + 2.5 LSB	–2.499810	0000 0000 0000 0010
AGND + 1.5 LSB	+0.000057	$-V_{REF}$ + 1.5 LSB	–2.499886	0000 0000 0000 0001
AGND + 0.5 LSB	+0.000019	$-V_{REF}$ + 0.5 LSB	–2.499962	0000 0000 0000 0000

NOTES

[1] V_{REF} = +2.5 V

[2] AGND = 0 V

[3] Unipolar Mode, 1 LSB = 2.5 V/655536 = 0.000038 V

[4] Bipolar Mode, 1 LSB = 5 V/65536 = 0.000076 V

[5] Inputs are voltages at code transitions.

INPUT SIGNAL CONDITIONING

Reference voltages from +1 V to +3 V may be used with the AD7701, with little degradation in performance. Input ranges that cannot be accommodated by this range of reference voltages may be achieved by input signal conditioning. This may take the form of gain to accommodate a smaller signal range, or passive attenuation to reduce a larger input voltage range.

Source Resistance

If passive attenuators are used in front of the AD7701, care must be taken to ensure that the source impedance is sufficiently low. The AD7701 has an analog input with over 1 GΩ dc input resistance. In parallel with this there as a small dynamic load which varies with the clock frequency (see Figure 13). Each time the analog input is sampled, a 10 pF capacitor draws a charge packet of maximum 1 pC (10 pF × 100 mV)

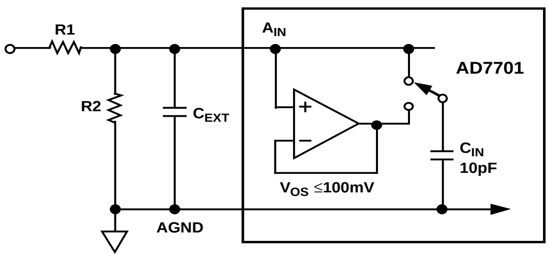


Figure 13. Equivalent Input Circuit and Input Attenuator

from the analog source with a frequency $f_{CLKIN}/256$. For a 4.096 MHz CLKIN, this yields an average current draw of 16 nA. After each sample the AD7701 allows 62 clock periods for the input voltage to settle. The equation which defines settling time is:

$$V_O = V_{IN} [1 - e^{-t/RC}]$$

where:

- V_O is the final settled value,
- V_{IN} is the value of the input signal,
- R is the value of the input source resistance,
- C is the 10 pF sample capacitor,
- t is equal to $62/f_{CLKIN}$.

From this, the following equation can be developed which gives the maximum allowable source resistance, $R_{S(MAX)}$, for an error of V_E:

$$R_{S(MAX)} = \frac{62}{f_{CLKIN} \times (10\,pF) \times ln(100\,mV / V_E)}$$

Provided the source resistance is less than this value, the analog input will settle within the desired error band in the requisite 62 clock periods. Insufficient settling leads to offset errors. These can be calibrated in system calibration schemes.

If a limit of 10 µV (0.25 LSB at 16 bits) is set for the maximum offset voltage, then the maximum allowable source resistance is 160 kΩ from the above equation, assuming that there is no external stray capacitance.

An RC filter may be added in front of the AD7701 to reduce high frequency noise. With an external capacitor added from A_{IN} to AGND, the following equation will specify the maximum allowable source resistance:

$$R_{S(Max)} = \frac{62}{f_{CLKIN} \times (C_{IN} + C_{EXT}) \times ln\left[\frac{100\,mV \times C_{IN} / (C_{IN} + C_{EXT})}{V_E}\right]}$$

The practical limit to the maximum value of source resistance is thermal (Johnson) noise. A practical resistor may be modeled as an ideal (noiseless) resistor in series with a noise voltage source or in parallel with a noise current source.

$$V_n = \sqrt{4\,kTRf}\ Volts$$

$$i_n = \sqrt{4\,kTf / R}\ Amperes$$

where:

k is Boltzmann's constant (1.38×10^{-23} J/K)

and

T is temperature in degrees Kelvin (°C + 273).

Active signal conditioning circuits such as op amps generally do not suffer from problems of high source impedance. Their open loop output resistance is normally only tens of ohms and, in any case, most modern general purpose op amps have sufficiently fast closed loop settling time for this not to be a problem. Offset voltage in op amps can be eliminated in a system calibration routine. With the wide dynamic range and small LSB size of the AD7701, noise can also be a problem, but the digital filter will reject most broadband noise above its cutoff frequency. However, in certain applications there may be a need for analog input filtering.

Antialias Considerations

The digital filter of the AD7701 does not provide any rejection at integer multiples of the sampling frequency ($nf_{CLKIN}/256$, where n = 1, 2, 3 . . .).

With a 4.096 MHz master clock there are narrow (±10 Hz) bands at 16 kHz, 32 kHz, 48 kHz, etc., where noise passes unattenuated to the output.

However, due to the AD7701's high oversampling ratio of 800 (16 kHz to 20 Hz) these bands occupy only a small fraction of the spectrum, and most broadband noise is filtered. The reduction in broadband noise is given by:

$$e_{OUT} = e_{IN} \sqrt{2 f_C / f_S} = 0.035\, e_{IN}$$

where:

- e_{IN} and e_{OUT} are rms noise terms referred to the input
- f_C is the filter –3 dB corner frequency ($f_{CLKIN}/409600$)

and

- f_S is the sampling frequency ($f_{CLKIN}/256$).

Since the ratio of f_S to f_{CLKIN} is fixed, the digital filter reduces broadband white noise by 96.5% independent of the master clock frequency.

VOLTAGE REFERENCE CONNECTIONS

The voltage applied to the V_{REF} pin defines the analog input range. The specified reference voltage is 2.5 V, but the AD7701 will operate with reference voltages from 1 V to 3 V with little degradation in performance.

The reference input presents exactly the same dynamic load as the analog input, but in the case of the reference input, source resistance and long settling time introduce gain errors rather than offset errors. Fortunately, most precision references have sufficiently low output impedance and wide enough bandwidth to settle to 10 µV within 62 clock cycles.

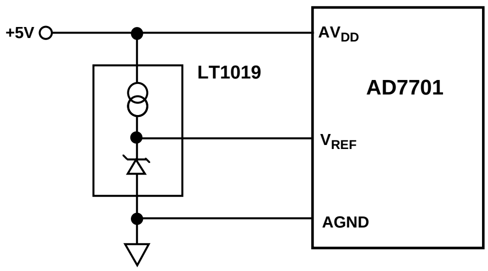


Figure 14. Typical External Reference Connections

The digital filter of the AD7701 removes noise from the reference input, just as it does with noise at the analog input, and the same limitations apply regarding lack of noise rejection at integer multiples of the sampling frequency. If reference noise is a problem, some voltage references offer noise reduction schemes using an external capacitor. Alternatively, a simple RC filter may be used, as shown in Figure 15.

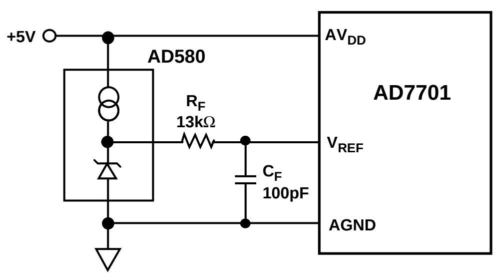


Figure 15. Filtered Reference Input

The same considerations apply to this filter as to a filter at the analog input. In this case:

$$[R_F(C_F+10\,pF)] = \frac{62}{f_{CLKIN}\times ln\left[\dfrac{100\,mV\times C_{IN}(C_{IN}+C_F)}{V_{FSE}}\right]}$$

where:

f_{CLKIN} is the master clock frequency

and

V_{FSE} is the maximum desired error in volts.

GROUNDING AND SUPPLY DECOUPLING

AGND is the ground reference voltage for the AD7701, and is completely independent of DGND. Any noise riding on the AGND input with respect to the system analog ground will cause conversion errors. AGND should therefore be used as the system ground and also as the ground for the analog input and the reference voltage.

The analog and digital power supplies to the AD7701 are independent and separately pinned out, to minimize coupling between analog and digital sections of the device. The digital filter will provide rejections of broadband noise on the power supplies, except at integer multiples of the sampling frequency. Therefore, the two analog supplies should be decoupled to AGND using 100 nF ceramic capacitors to provide power supply noise rejections at these frequencies. The two digital supplies should similarly be decoupled to DGND.

ACCURACY AND AUTOCALIBRATION

Sigma-delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no-missing-codes performance. The AD7701 achieves excellent linearity (±0.0007%) by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient.

The AD7701 offers two self-calibration modes using the on-chip calibration microcontroller and SRAM. Table III is a truth table for the calibration control inputs SC1 and SC2.

In the self-calibration mode, zero-scale is calibrated against the AGND pin and full scale is calibrated against the V_{REF} pin, to remove internal errors.

Note that in the bipolar mode the AD7701 calibrates positive full scale and midscale (bipolar zero).

In the system-calibration mode, the AD7701 calibrates its zero and full scale to voltages present on the analog input pin in two sequential steps. This allows system offsets and/or gain errors to be nulled out.

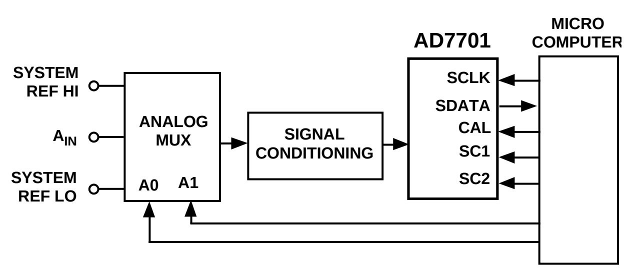


Figure 16. Typical Connections for System Calibration

A typical system calibration scheme is shown in Figure 16. In normal operation the analog signal is fed to the AD7701 via an analog multiplexer. When the system is to be calibrated, A_{IN} is first switched to the system REF LO via the multiplexer and CAL is strobed high, with SC1 and SC2 both high. AIN is then switched to the system REF HI and CAL is strobed, with SC1 low and SC2 high. In this way, the effect of all error sources

Table III. Calibration Truth Table

CAL	SC1	SC2	CAL TYPE	ZERO REFERENCE	FS REFERENCE	SEQUENCE	CALIBRATION TIME
⎍	0	0	Self-Cal	AGND	V_{REF}	One Step	3,145,655 Clock Cycles
⎍	1	1	System Offset	A_{IN}	–	1st Step	1,052,599 Clock Cycles
⎍	0	1	System Gain	–	A_{IN}	2nd Step	1,068,813 Clock Cycles
⎍	1	0	System Offset	A_{IN}	V_{REF}	One Step	2,117,389 Clock Cycles

NOTE
$\overline{DRDY}$ remains high throughout the calibration sequence. In the Self-Cal mode, $\overline{DRDY}$ falls once the AD7701 has settled to the analog input. In all other modes $\overline{DRDY}$ falls as the device begins to settle.

between the multiplexer and the AD7701 is removed. Op amps and other signal conditioning circuits may be used in front of the AD7701, without worrying about their absolute gain or offset errors. Note that the absolute value of the reference supplied to the AD7701 is no longer important, provided it has adequate short-term stability between calibration cycles, as full scale is calibrated to the system reference.

If system offset errors are important but system gain errors are not, then a one step system calibration may be performed with SC1 high and SC2 low. In this case, offset is calibrated against A_{IN}, which should be connected to system REF LO during calibration, but full scale is calibrated against the AD7701's V_{REF} input.

System calibration schemes will yield better accuracy than self-calibration, even if there are no system errors. Using self-calibration, errors arise due to the mismatch in source impedances between the references during calibration (AGND and V_{REF}) and the analog input during normal operation. In system calibration, the source impedances inherently remain identical, such that the theoretical limit to system accuracy is calibration resolution. The practical limit is the noise floor of the AD7701.

Note that in system calibration, "REF LO" does not necessarily mean the system ground or zero volts. The AD7701 can be calibrated to measure between any two voltages that lie within its calibration range by deliberately making REF LO nonzero. For example, if REF LO is +0.5 V and REF HI is +2.5 V, the unipolar span will be between these limits.

CALIBRATION RANGE

When designing system calibration schemes, care must be taken to ensure that the worst-case system errors do not cause the overrange headroom of the AD7701 to be exceeded. Although the measurement error caused by offset and gain errors can be nulled out, the actual error voltages will still be present at the analog input and can cause overloading of the analog modulator or overflow of the digital filter. With a 2.5 V reference, the maximum input voltage is ($+V_{REF}$ + 100 mV), and the minimum input voltage is ($-V_{REF}$ – 100 mV).

POWER-UP AND CALIBRATION

A calibration cycle must be carried out after power-up to initialize the device to a consistent starting condition and correct calibration. The CAL pin must be held high for at least four clock cycles, after which calibration is initiated on the falling edge of CAL and takes a maximum of 3,145,655 clock cycles (approximately 768 ms, with a 4.096 MHz clock). See Table III.

The type of calibration cycle initiated by CAL is determined by the SC1 and SC2 inputs, in accordance with Table III.

The power dissipation and temperature drift of the AD7701 are low and no warm-up time is required before the initial calibration is performed. However, the system reference must have stabilized before calibration is initiated.

POWER SUPPLY SEQUENCING

The positive digital supply (DV_{DD}) must never exceed the positive analog supply (AV_{DD}) by more than 0.3 V. Power supply sequencing is therefore important. If separate analog and digital supplies are used, care must be taken to ensure that the analog supply is powered up first.

It is also important that power is applied to the AD7701 before signals at V_{REF}, A_{IN} or the logic input pins in order to avoid any possibility of latch-up. If separate supplies are used for the AD7701 and the system digital circuitry, then the AD7701 should be powered up first.

A typical scheme for powering the AD7701 from a single set of ±5 V rails is shown in the system connection diagram, Figure 7. In this circuit AV_{DD} and DV_{DD} are brought along separate tracks from the same +5 V supply. Thus, there is no possibility of the digital supply coming up before the analog supply.

GROUNDING

The AD7701 uses the analog ground connection, AGND, as the measurement reference node. It should be used as the reference node for both the analog input signal and the reference voltage at the V_{REF} pin.

The analog and digital power supplies to the AD7701 die are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled separately to their respective grounds as shown in Figure 7. The on-chip digital filtering of the AD7701 further enhances power supply rejection by attenuating noise injected into the conversion process.

SINGLE SUPPLY OPERATION

Figure 17 shows a circuit to power the AD7701 from a single +10 V supply, using an op amp to provide a half supply reference point for AGND and DGND. As the digital I/O pins are referenced to this point, level shifting is required for external digital communications. If galvanic isolation is required in the system, level shifting and isolation can both be provided by opto-isolators.

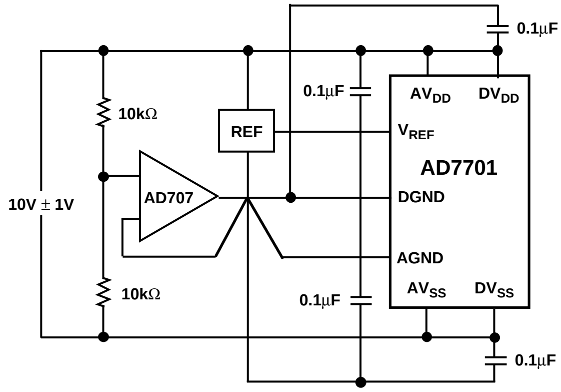


Figure 17. Single Supply Operation

SLEEP MODE

The low power standby mode is initiated by taking the $\overline{\text{SLEEP}}$ input low, which shuts down all analog and digital circuits and reduces power consumption to 10 µW. The calibration coefficients are still retained in memory, but as the converter has been quiescent, it is necessary to wait for the filter settling time (507,904 cycles) before accessing the output data.

DIGITAL INTERFACE

The AD7701's serial communications port allows easy interfacing to industry-standard microprocessors. Three different modes of operations are available, optimized for different types of interface.

SYNCHRONOUS SELF-CLOCKING MODE (SSC)

The SSC mode (MODE pin high) allows easy interfacing to serial-parallel conversion circuits in systems with parallel data communication. This mode allows interfacing to 74XX299 Universal Shift registers without any additional decoding. The SSC mode can also be used with microprocessors such as the 68HC11 and 68HC05, which allow an external device to clock their serial port.

Figure 18 shows the timing diagram for the SSC mode. Data is clocked out by an internally generated serial clock. The AD7701 divides each sampling interval into sixteen distinct periods. Eight periods of 64 clock pulses are for analog settling and eight periods of 64 clock pulses are for digital computation. The status of $\overline{\text{CS}}$ is polled at the beginning of each digital computation period. If it is low at any of these times then SCLK will become active and the data word currently in the output register will be transmitted, MSB first. After the LSB has been transmitted $\overline{\text{DRDY}}$ goes high and SDATA goes three-state. If $\overline{\text{CS}}$, having been brought low, is taken high again at any time during data transmission, SDATA and SCLK will go three-state after the current bit finishes. If $\overline{\text{CS}}$ is subsequently brought low, transmission will resume with the next bit during the subsequent digital computation period. If transmission has not been initiated and completed by the time the next data word is available, $\overline{\text{DRDY}}$ will go high for four clock cycles then low again as the new word is loaded into the output register.

A more detailed diagram of the data transmission in the SSC mode is shown in Figure 19. Data bits change on the falling edge of SCLK and are valid on the rising edge of SCLK.

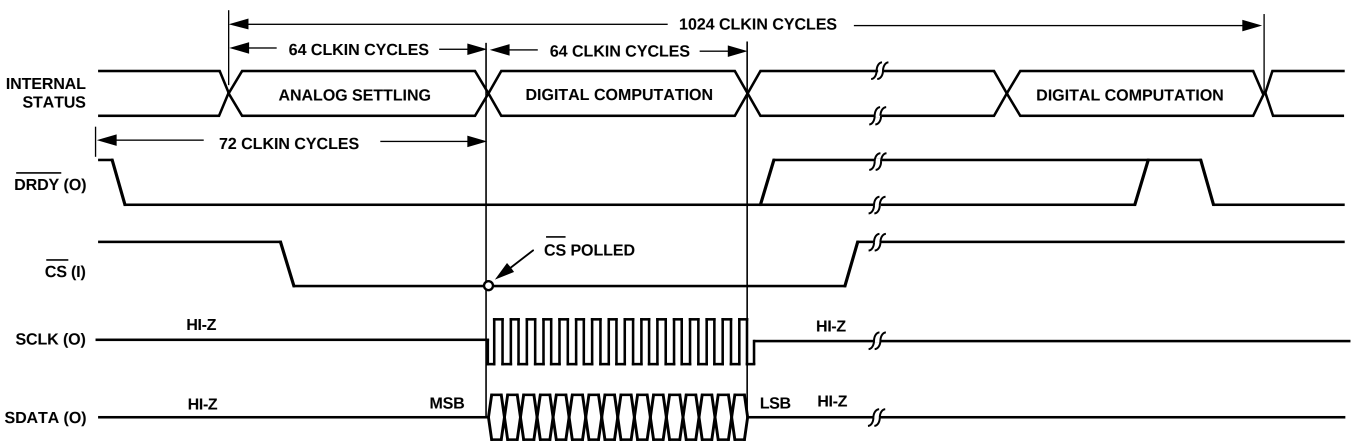


Figure 18. Timing Diagram for SSC Data Transmission Mode

SYNCHRONOUS EXTERNAL CLOCK MODE (SEC)

The SEC mode (MODE pin grounded) is designed for direct interface to the synchronous serial ports of industry-standard microprocessors such as the COPS series, 68HC11 and 68HC05. The SEC mode also allows customized interfaces, using I/O port pins, to microprocessors that do not have a direct fit with the AD7701's other modes.

As shown in Figure 20, a falling edge on $\overline{CS}$ enables the serial data output with the MSB initially valid. Subsequent data bits change on the falling edge of an externally supplied SCLK. After the LSB has been transmitted, $\overline{DRDY}$ goes high and SDATA goes three-state. If $\overline{CS}$ is low and the AD7701 is still transmitting data when a new data word becomes available, the old data word continues to be transmitted and the new data is lost.

If $\overline{CS}$ is taken high at any time during data transmission, SDATA and SCLK will go three-state immediately. If $\overline{CS}$ returns low, the AD7701 will continue transmission with the same data bit. If transmission has not been initiated and completed by the time the next data word becomes available, and if $\overline{CS}$ is high, $\overline{DRDY}$ will return high for four clock cycles, then fall as the new word is loaded into the output register.

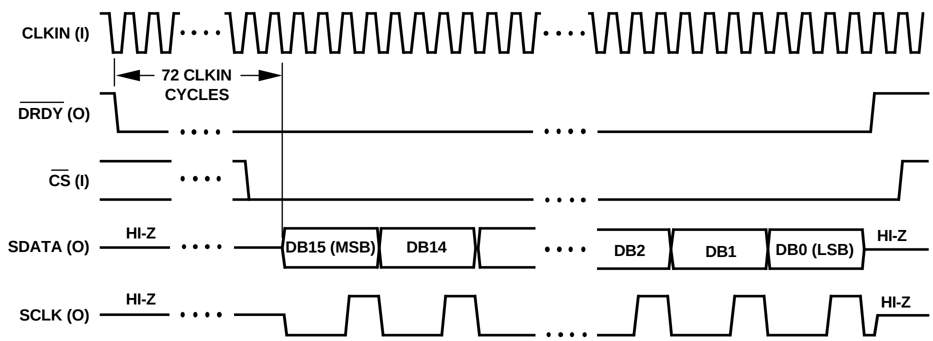


Figure 19. SSC Mode Showing Data Timing Relative to SCLK

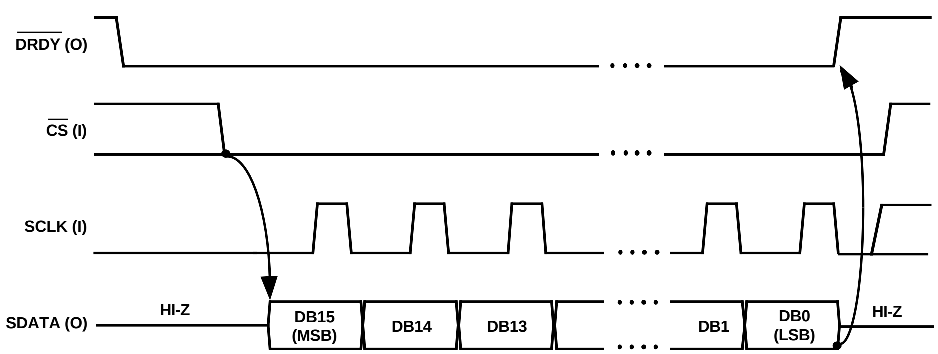


Figure 20. Timing Diagram for the SEC Mode

ASYNCHRONOUS COMMUNICATIONS (AC) MODE

The AC mode (MODE pin tied to –5 V) offers a UART-compatible interface which allows the AD7701 to transmit data asynchronously from remote locations. An external SCLK sets the baud rate and data is transmitted in two bytes in UART-compatible format. Using the AC mode, the AD7701 can be interfaced direct to microprocessors with UART interfaces, such as the 8051 and TMS70X2.

Data transmission is initiated by $\overline{CS}$ going low. If $\overline{CS}$ is low on a falling edge of SCLK, the AD7701 begins transmitting an 8-bit data byte (DB8–DB15) with one start bit and two stop bits, as in Figure 21. The SDATA output will then go three-state. The second byte is transmitted by bringing $\overline{CS}$ low again and DB0 to DB7 are transmitted in the same format as the first byte.

UART baud rates are typically low compared to the AD7701's 4 kHz output update rate. If $\overline{CS}$ is low and data is still being transmitted when a new data word becomes available, the new data will be ignored. However, if $\overline{CS}$ has been taken high between bytes, when a new data word becomes available, the AD7701 could update the output register before the second byte is transmitted. In this case, the UART would receive the first byte of the new word instead of the second byte of the old word. When using the AC mode, care must obviously be taken to ensure that this does not occur.

DIGITAL NOISE AND OUTPUT LOADING

As mentioned earlier, the AD7701 divides its internal timing into two distinct phases, analog sampling and settling and digital computation. In the SSC mode, data is transmitted only during the digital computation periods, to minimize the effects of digital noise on analog performance. In the SEC and AC modes data transmission is externally controlled, so this automatic safeguard does not exist.

Whatever mode of operation is used, resistive and capacitive loads on digital outputs should be minimized in order to reduce crosstalk between analog and digital portions of the circuit. For this reason connection to low-power CMOS logic such as one of the 4000 series or 74C families is recommended.

It is especially important to minimize the load on SDATA in the AC mode, as transmission in this mode is inherently asynchronous. In the SEC mode the AD7701 should be synchronized to the digital system clock via CLKIN.

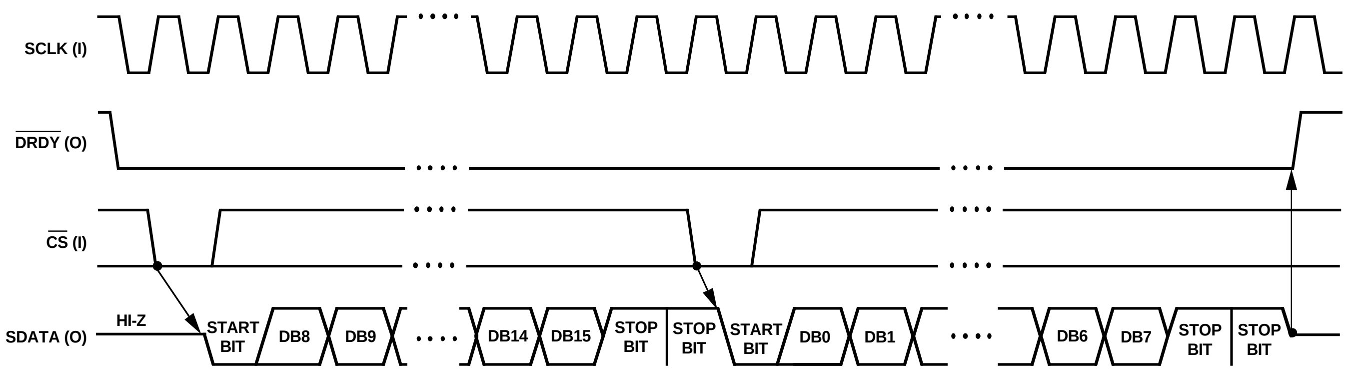
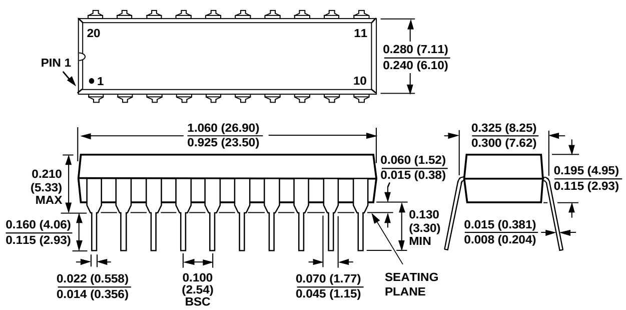


Figure 21. Timing Diagram for Asynchronous Communications Mode

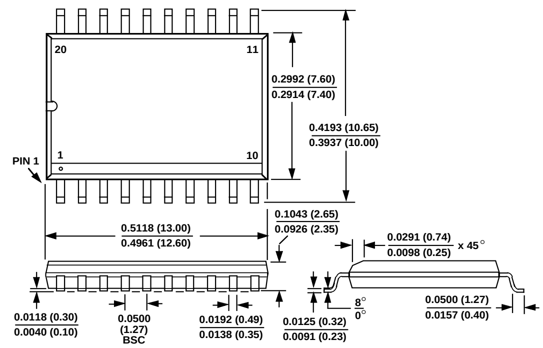
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

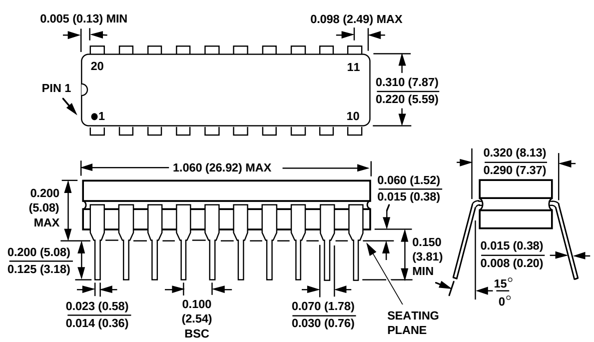
20-Pin Plastic DIP (N-20)



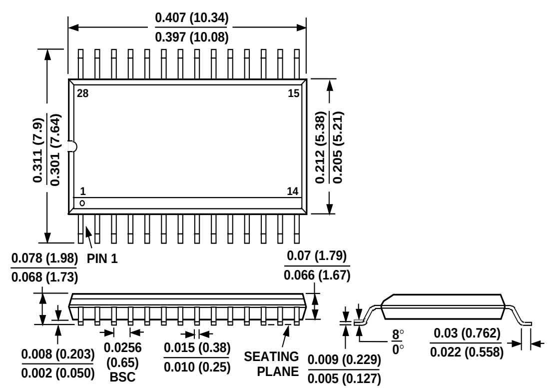
20-Lead SOIC (R-20)



20-Pin Cerdip (Q-20)



28-Lead SSOP (RS-28)



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